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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/508,816	08/10/2005	Robert Denk	LLP141WOUS	5934

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EXAMINER	
WENDELL, ANDREW	

ART UNIT	PAPER NUMBER
2618	

DATE MAILED: 09/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/508,816	DENK ET AL.	
	Examiner	Art Unit	
	Andrew Wendell	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *15 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 9-20 rejected under 35 U.S.C. 102(b) as being anticipated by Hirata (US Pat# 5,920,557).

Regarding claim 9, Hirata's synchronizing circuit teaches producing an internal actual transmission time signal in the transmitting/receiving unit, containing information about an actual transmission time (Col.3 lines 8-12), comparing 4 (Fig. 2) the internal actual transmission time signal with an external nominal transmission time signal which is received at the transmitting/receiving unit and which contains information about a nominal transmission time (Col. 3 lines 8-13), producing a difference signal in the transmitting/receiving unit, which contains information about a discrepancy between the two transmission times associated with the actual and nominal transmission time signals, and correcting B (Fig. 2) the actual transmission time is in the transmitting/receiving unit such that the discrepancy between the two transmission times, contained in the difference signal, is minimized, wherein the correction is carried out independently of a defined clock 8 (Fig. 2) period of the transmitting/receiving unit, and wherein a time period for the correction is set variably therein, and wherein a time duration of the correction is set by a value of a conversion ratio of a fractional sampling

of an input data signal, and of a time duration for which this conversion ratio is activated (Col. 3 lines 6-Col. 5 line 24).

Regarding claim 10, Hirata teaches wherein the discrepancy between the transmission times is minimized such that the input data signal is compressed or extended in time (Col. 3 lines 6-Col. 5 line 24).

Regarding claim 11, Hirata teaches wherein the input data signal is compressed or extended in time by reducing or increasing the conversion ratio of the fractional sampling performed on the input data signal (Col. 3 lines 6-Col. 5 line 24).

Regarding claim 12, Hirata teaches wherein correcting the actual transmission time comprises applying a correction signal to a fractional sampling rate converter unit to change the conversion ratio associated therewith such that the conversion ratio is set either to a value which is predetermined and fixed for a steady-state system, or to a value which corresponds to the extension or compression of the input data signal (Col. 3 lines 6-Col. 5 line 24).

Regarding claim 13, Hirata teaches wherein the correction signal contains, as information, a value to which the conversion ratio is changed, a time period for which the changed conversion ratio is used, and a time at which the changed conversion ratio is activated (Col. 3 lines 6-Col. 5 line 24).

Regarding claim 14, Hirata teaches deactivating the correction signal if the time discrepancy is less than a threshold value, and setting the conversion ratio to a value defined for the steady state (Col. 3 lines 6-Col. 5 line 24).

Regarding claim 15, Hirata teaches wherein the input data signal is compressed or extended in time such that no information is removed from or added to the input data signal (Col. 3 lines 6-Col. 5 line 24).

Regarding claim 16, Hirata teaches wherein the actual transmission time is corrected over various clock domains of the transmitting/receiving unit, which have different or identical clock durations, and the external nominal transmission time signal is generated in a clock domain which is different to the clock domain which is clocked by the working clock, and which is not synchronous therewith (Col. 3 lines 6-Col. 5 line 24).

Regarding claim 17 Hirata teaches a control signal by means of which the working clock in the transmitting/receiving unit is controlled (Col. 3 lines 6-Col. 5 line 24).

Regarding claim 18, Hirata teaches counting edges of a working clock signal in order to determine the actual transmission time (Col. 3 lines 6-Col. 5 line 24, used in TDMA).

Regarding claim 19, Hirata teaches wherein the actual transmission time signal is produced based on the determined actual transmission time (Col. 3 lines 6-Col. 5 line 24).

Regarding claim 20, Hirata teaches resetting periodically (could be any amount of time) the counting when the transmitting/receiving unit is in the steady state, with a period duration of the nominal transmission time signal (Col. 3 lines 6-Col. 5 line 24).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 4-5, 8 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata (US Pat# 5,920,557) in view of Scott (US Pat# 6,388,997).

Regarding claim 1, Hirata's synchronizing circuit teaches a correction unit B configured to produce an output data signal based on a received correction signal, a sequence control 9 (Fig. 2) unit connected downstream from the correction unit B (Fig. 2) and configured to produce a working clock signal, a counter unit 5 (Fig. 2) electrically connected to the sequence control unit 9 (Fig. 2) and a control device A (Fig. 2) configured to compare the internal actual transmission time signal with an external nominal transmission time signal to produce the correction signal, and further configured to transmit the correction signal to the correction unit in order to correct the actual transmission time (Col. 3 lines 6-27). Hirata fails to teach a counter using a working clock signal from a sequence control unit.

Scott's timing adjustment control for efficient time division duplex communication teaches a counter unit 911 (Fig. 9) electrically connected to the sequence control unit 906 (Fig. 9) and configured to use the working clock signal from the sequence control unit 906(Fig. 9) to generate an internal actual transmission time signal (Col. 19 line 57-Col. 20 line 32).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a counter using a working clock signal from a sequence control unit as taught by Scott into Hirata's synchronizing circuit in order to improve efficiency of the system (Col. 4 lines 20-37).

Regarding claim 2, the combination including Hirata teaches wherein the control device has comprises a comparator unit 4 (Fig. 2) configured to compare the actual transmission time signal with the nominal transmission time signal, and produce a difference signal from a discrepancy between two transmission times associated with the actual and nominal transmission time signals (Col. 3 lines 8-17).

Regarding claim 4, the combination including Hirata teaches wherein the control device comprises a time control unit 1 (fig. 2) connected upstream of the comparator unit 4 (Fig. 2) and configured to transmit the external nominal transmission time signal to the comparator unit.

Regarding claim 5, the combination including Hirata teaches wherein the correction unit comprises a fractional sampling rate converter unit with a variable conversion ratio (Col. 3 lines 6-Col. 5 line 24).

Regarding claim 8, the combination including Scott teaches wherein the transmitting/receiving station comprises a mobile station which supports one of the standards UMTS or GSM (Col. 3 line 27-Col. 4 line 14).

Regarding claim 21, the combination including Scott teaches wherein the transmitting/receiving unit comprises a mobile station, and supports a UMTS or GSM mobile radio standard (Col. 3 line 27-Col. 4 line 14).

3. Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata (US Pat# 5,920,557) in view of Scott (US Pat# 6,388,997) as applied to claims 1-2 above, and further in view of Kada et al. (US Pat# 6,687,321).

Regarding claim 3, Hirata's synchronizing circuit in view of Scott's timing adjustment control for efficient time division duplex communication teaches the limitations in claims 1-2. Both Hirata and Scott fail to teach a control unit connected downstream from the comparator unit.

Kada et al. circuit teaches wherein the control device comprises a control unit 24 (Fig. 1) connected downstream from the comparator unit 23 (Fig. 1) and configured to use the difference signal generated by the comparator unit from the comparison of the actual transmission time signal with the nominal transmission time signal, to produce the correction signal (Col. 4 lines 23-28).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a control unit connected downstream from the comparator unit as taught by Kada et al. into a counter using a working clock signal from a sequence control unit as taught by Scott into Hirata's synchronizing circuit in order to improve the accuracy of communication (Col. 2 lines 47-63).

Regarding claim 6, Kada further teaches a signal processing unit 20 (Fig. 1) for configured to produce an input data signal connected downstream from the counter unit 12 (Fig. 1) and from the sequence control unit 13 (Fig. 1), and connected upstream of the sampling rate converter unit 22 (Fig. 1).

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi et al. (US Pat Appl# 2004/0152438) in view of Hirata (US Pat# 5,920,557) as applied to claim 1 above, and further in view of Partyka (US Pat Appl# 2003/0174757).

Regarding claim 7, Hirata's synchronizing circuit in view of Scott's timing adjustment control for efficient time division duplex communication teaches the limitations in claim 1. Both Hirata and Scott fail to teach a D/A converter.

Partyka's circuit teaches a D/A converter (has to be some D/A converter since there are two A/D converters 122 and 124 of Fig. 2) configured to produce an analog transmission signal as a function of the output data signal and of a sampling clock signal from a sampling clock source (Sections 0007-0013).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a D/A converter as taught by Partyka into a counter using a working clock signal from a sequence control unit as taught by Scott into Hirata's synchronizing circuit in order to converse battery power and maintain synchronization with communication devices (Sections 0006 and 0007).

Response to Arguments

5. Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Wendell whose telephone number is 571-272-0557. The examiner can normally be reached on 7:30-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nay Maung can be reached on 571-272-7882. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Andrew Wendell
Examiner
Art Unit 2618

9/7/2006

Quochien Ba Vuong 9/15/06
QUOCHIEN B. VUONG
PRIMARY EXAMINER